REMARKS

Claims 1-23 are rejected. Claims 1-23 are currently pending. Applicants respectfully request further examination and reconsideration in view of the remarks set forth below. Applicants believe that the amendments herein to the patent application do not add new matter to it.

35 U.S.C. §103 Rejections

Claims 1-23 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Hashimoto et al., U.S. Patent No. 6,983,374 (hereinafter Hashimoto), in view of Ellison et al., U.S. Patent No. 7,082,615 (hereinafter Ellison), and further in view of Kittirutsunetorn, U.S. Patent No. 5,081,675 (hereinafter Kittirutsunetorn).

Claims 1-11

Applicants respectfully direct the Examiner to amended independent Claim 1 (emphasis added):

> A memory architecture, comprising:
>
> an unprotected memory space configured to store encrypted information, said encrypted information corresponding to a plain text version thereof, said unprotected memory space is located outside a microprocessor;
>
> a message digest corresponding to said encrypted information;
>
> a first protected memory space configured to store at least a subset of operating system instructions, said first protected memory space is located outside said microprocessor; and
>
> a second protected memory space configured to store said plain text version of said encrypted information, said second protected memory space is located outside said microprocessor;
>
> wherein said operating system instructions in said first protected memory space operate on said plain text version of said encrypted information in said second protected memory space;
>
> wherein a random access memory comprises said unprotected memory space, said first protected memory space, and said second protected memory space.

Applicants respectfully assert that Hashimoto does not teach or suggest "said unprotected memory space is located outside a microprocessor; . . . said first protected

memory space is located outside said microprocessor; . . . said second protected memory space is located outside said microprocessor" as specifically recited in amended independent Claim 1. Moreover, Applicants respectfully contend that Hashimoto actually teaches away from "said unprotected memory space is located outside a microprocessor; . . . said first protected memory space is located outside said microprocessor; . . . said second protected memory space is located outside said microprocessor" as specifically recited in amended Claim 1.

Therefore, since Hashimoto is solely relied upon to teach the above discussed elements and since Hashimoto fails to teach or suggest these elements as recited in amended independent Claim 1, Applicants respectfully submit that amended independent Claim 1 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

Applicants respectfully point out that Claims 2-11 depend from allowable amended independent Claim 1 and recite further patentable subject matter. Therefore, Applicants respectfully submit that Claims 2-11 are thus in condition for allowance for at least being dependent on an allowable base claim.

Claims 12-16

Applicants respectfully direct the Examiner to amended independent Claim 12 (emphasis added):

> A system for operating on encrypted information, comprising:
> a microprocessor; and
> a memory architecture of comprising:
> an unprotected memory space configured to store encrypted information, said encrypted information corresponding to a plain text version thereof, said unprotected memory space is located outside said microprocessor;
> a message digest corresponding to said encrypted information;
> a first protected memory space configured to store at least a subset of operating system instructions, said first protected memory space is located outside said microprocessor; and

a second protected memory space configured to store said plain text version of said encrypted information, said second protected memory space is located outside said microprocessor, wherein said operating system instructions in said first protected memory space operate on said plain text version of said encrypted information in said second protected memory space;

wherein said microprocessor is configured to execute said operating system instructions;

wherein a hard drive comprises said unprotected memory space, said first protected memory space, and said second protected memory space.

Applicants respectfully contend that Hashimoto fails to teach or suggest "said unprotected memory space is located outside a microprocessor; . . . said first protected memory space is located outside said microprocessor; . . . said second protected memory space is located outside said microprocessor" as explicitly recited in amended independent Claim 12. Furthermore, Applicants respectfully contend that Hashimoto actually teaches away from "said unprotected memory space is located outside a microprocessor; . . . said first protected memory space is located outside said microprocessor; . . . said second protected memory space is located outside said microprocessor" as specifically recited in amended Claim 12.

Therefore, since Hashimoto is solely relied upon to teach the above discussed elements and since Hashimoto fails to teach or suggest these elements as recited in amended independent Claim 12, Applicants respectfully submit that amended independent Claim 12 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

Applicants respectfully point out that Claims 13-16 depend from allowable amended independent Claim 12 and recite further patentable subject matter. Therefore, Applicants respectfully submit that Claims 13-16 are thus in condition for allowance for at least being dependent on an allowable base claim.

Claims 17-21

Applicants respectfully direct the Examiner to amended independent Claim 17 (emphasis added):

> A method of operating on encrypted information, comprising:
> transferring said encrypted information to a first protected memory address inaccessible to a user-accessible software program, but accessible to an operating system instruction set, said first protected memory address is located outside a microprocessor;
> if said encrypted information comprises encrypted information, decrypting said encrypted information to form a decrypted version of said encrypted information, said decrypting comprises a message digest; and
> storing said first protected memory address in a second protected memory address inaccessible to a user-accessible software program, but accessible to an operating system instruction set, wherein said second protected memory address is linked to an original location of said encrypted information, said second protected memory address is located outside said microprocessor;
> wherein a detachable electronically erasable and programmable memory comprises said first protected memory address and said second protected memory address.

Applicants respectfully assert that Hashimoto fails to teach or suggest "said first protected memory address is located outside a microprocessor; . . . said second protected memory address is located outside said microprocessor" as specifically recited in amended independent Claim 17. Additionally, Applicants respectfully contend that Hashimoto actually teaches away from "said first protected memory address is located outside a microprocessor; . . . said second protected memory address is located outside said microprocessor" as explicitly recited in amended Claim 17.

Therefore, since Hashimoto is solely relied upon to teach the above discussed elements and since Hashimoto fails to teach or suggest these elements as recited in amended independent Claim 17, Applicants respectfully submit that amended independent Claim 17 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

Applicants respectfully point out that Claims 18-22 depend from allowable amended independent Claim 17 and recite further patentable subject matter. Therefore, Applicants respectfully submit that Claims 18-22 are thus in condition for allowance for at least being dependent on an allowable base claim.

Claim 23

Applicants respectfully direct the Examiner to amended independent Claim 23 (emphasis added):

> A system for hiding information, comprising:
> one or more units of information to be hidden;
> a unique identifier for each of said units of information;
> one or more tools configured to hide each of the units of information at a known location in protected memory, said protected memory is located outside a microprocessor; and
> a second location in said protected memory for storing each of said unique identifiers and a corresponding known location in protected memory where the corresponding unit of information is hidden;
> wherein an optical data storage medium comprises said protected memory.

Applicants respectfully contend that Hashimoto does not teach or suggest "one or more tools configured to hide each of the units of information at a known location in protected memory, said protected memory is located outside a microprocessor" as specifically recited in amended independent Claim 23. Additionally, Applicants respectfully contend that Hashimoto actually teaches away from "said protected memory is located outside a microprocessor" as explicitly recited in amended Claim 23.

Therefore, since Hashimoto is solely relied upon to teach the above discussed elements and since Hashimoto fails to teach or suggest these elements as recited in amended independent Claim 23, Applicants respectfully submit that amended independent Claim 23 overcomes the rejections under 35 U.S.C. §103(a), and is thus in condition for allowance.

CONCLUSION

For all the reasons advanced above, Applicants respectfully submit that pending Claims 1-23 are in condition for allowance and that action is respectfully solicited.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any required fees or credit any overpayments to Deposit Account Number: 50-4160.

Respectfully submitted,

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Dated: AUG. 14, 2008

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